Atty. Docket No. OPP-GZ-2007-0022-US
Serial No: 10/736,063

Remarks

Applicant and his representatives wish to thank Examiner Mitchell for the thorough examination of the present application and the detailed explanations in the Office Action dated February 21, 2007. The specification has been amended to fix a typographical error. Claim 1 has been amended to include the limitations of Claim 12. Support for new Claim 24 can be found in paragraphs **[0015]** and **[0018]** of the specification and FIG. 1c as originally filed. Support for new Claim 25 can be found in paragraphs **[0015]** and **[0019]** of the specification as originally filed. Thus, no new matter is introduced by the present Amendment.

The present invention relates to a method of forming gates in a semiconductor device. The method (as set forth in Claim 1 above) comprises:

(a) forming a shallow trench isolation (STI) to define an active region in a semiconductor substrate;

(b) forming a gate oxide layer on the semiconductor substrate;

(c) depositing a sacrificial layer on the semiconductor substrate to a thickness that determines a width of the gates;

(d) selectively etching the sacrificial layer to form a sidewall opening over the active region of the semiconductor substrate and the STI until the gate oxide is exposed;

(e) forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

(f) anisotropically etching the polycrystalline silicon layer such that the gates remain on sidewalls of the sidewall opening, the gates having the width; and

(g) removing the sacrificial layer.

The cited references neither disclose nor suggest a method of forming a gate in a semiconductor device, including depositing a sacrificial layer on the semiconductor substrate to a thickness that determines a width of the gates and selectively etching the sacrificial layer to form

a sidewall opening over the active region of the semiconductor substrate and the STI until the gate oxide is exposed (see elements (c) and (d) above).

The Rejection of Claims 1-12 and 16-23 under 35 U.S.C. § 102(e)

The rejection of Claims 1-12 and 16-23 under 35 U.S.C. § 102(e) as being anticipated by Kadosh et al. (US 6,383,872 [hereinafter "Kadosh"]) is respectfully traversed.

Kadosh discloses a semiconductor substrate 30, an isolation structure 34, a gate oxide 32 grown on the semiconductor substrate exclusive of the isolation structure, and a sacrificial material 36 deposited entirely across the gate oxide (see, e.g., col. 6, ll. 52-56, 63-64; and FIGS. 3-4). Kadosh further discloses blanket depositing a gate conductor material 40 across the upper surfaces 42 and the sidewall surfaces 44 in addition to it being deposited across the gate oxide and isolation structure (see, e.g., col. 7, ll. 6-10; and FIG. 5). Kadosh also discloses the thickness by which ***gate conductor material 40*** is deposited can vary depending on the amount of lateral extension needed from sidewall surfaces 44 to form an ensuing gate conductor, and that the greater the thickness, the greater the physical channel length might be (see, e.g., col. 7, ll. 10-16; and FIG. 5-6). Kadosh further discloses removing sacrificial structures 38 by a selective removal process (see, e.g., col. 7, ll. 46-49).

However, Kadosh is silent with regard to depositing **a sacrificial layer** on the semiconductor substrate to a thickness that determines a width of the gates, as recited in Claim 1 (see also, e.g., para. [0015], ll. 4-8; para. [0017], ll. 1-4; para. [0018], ll. 9-10; para [0020], ll. 1-2 of the present specification). As a result, it is believed the rejection of Claim 1 under 35 U.S.C. § 102(e) as being anticipated by Kadosh should be withdrawn.

Claims 2-12 and 16-23 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 2-12 and 16-23 are not anticipated by Kadosh for essentially the same reasons as Claim 1.

The Rejection of Claim 1 under 35 U.S.C. § 103(a)

The rejection of Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Hanafi et al. (US 2002/0197810 [hereinafter "Hanafi"]) in combination with Abeln et al. (US 6,207,510 [hereinafter "Abeln"]) and Rhodes (US 2004/0094784) is respectfully traversed.

Hanafi discloses a gate structure as shown in FIG. 15. Hanafi further discloses a double-spacer process preformed where first spacers 27 are insulators and second spacers 28 are materials from which the outer gate portions of the variable work function transistor would be formed (see, e.g., pg. 4, para. [0056], ll. 1-5; and FIG. 15). Hanafi also discloses that the formation of the second spacers define the width of the gate portions of the transistor; specifically, the distance between the second spacers delimits the width of the inner gate portion, and the width of the second spacers themselves respectively delimits the widths of the outer gate portions (see, e.g., pg. 4, para. [0057], ll. 1-8; and FIGS. 15-16).

Hanafi is deficient with regard to selectively etching a sacrificial layer having a thickness that determines a width of the gates to form a sidewall opening over the active region of the semiconductor substrate **and** the STI until the gate oxide is exposed, as recited in Claim 1. In fact, Hanafi is saliently deficient with regard to a STI region. As a result, Hanafi does not disclose or suggest all of the limitations of the present Claim 1.

Abeln discloses a semiconductor substrate 40 including at least one n-channel region 42 and a p-channel region 44 (see, e.g., col. 4, ll. 8-12; and FIG. 2). Like Hanafi, Abeln appears to be silent with regard to selectively etching a sacrificial layer having a thickness that determines a width of the gates to form a sidewall opening over the active region of the semiconductor substrate **and** the STI until the gate oxide is exposed, as recited in Claim 1. Therefore, Abeln does not cure the deficiencies of Hanafi with regard to Claim 1. As a result, the method of Claim 1 is patentable over Hanafi in view of Abeln.

Rhodes discloses forming p-type doped layer 120 in areas of substrate 110 and forming n-type region 126 directly beneath the active area of the pixel cell (see, e.g., pg. 4, para. [0040], ll. 2-3; para. [0041], ll. 1-5; and FIG. 3). Rhodes appears to be silent with regard to selectively

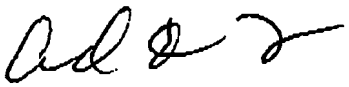
etching a sacrificial layer having a thickness that determines a width of the gates to form a sidewall opening over the active region of the semiconductor substrate **and** the STI until the gate oxide is exposed, as recited in Claim 1. As a result, no combination of Hanafi, Abeln, and Rhodes can disclose or suggest all of the limitations of the present Claim 1, and the rejection under 35 U.S.C. § 103(a) as being unpatentable over Hanafi in combination with Abeln and Rhodes should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases of rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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